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12EC027

M.Tech. Degree Examination, June/July 2014
Design of VLSI Systems

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- 1 a. With examples clearly define different description domains and levels of design abstraction. (05 Marks)
b. Explain the operation of Actel I/O pad with a neat circuit diagram. (05 Marks)
c. Describe different synthesis options available in chip design methods. (10 Marks)
- 2 a. How is simulation performed at different levels of abstraction in CMOS VLSI design? (10 Marks)
b. With flow chart, explain the sequence of steps to design a VLSI chip, with reframe to logical and physical design. (10 Marks)
- 3 a. Explain how multiplication is performed using radix-4 Booth encoding. Explain it with the help of Booth encoder and selector diagram. (10 Marks)
b. Draw a carry chain adder circuit built from switch logic using propagate, generate and kill signals. (05 Marks)
c. Explain unsigned magnitude comparator operation with circuit diagram and implementation table. (05 Marks)
- 4 a. With the help of 6 transistor RAM cell explain memory read and write operations. Also give relevant graphs for the same. (10 Marks)
b. Sketch the 4-bit LFSR for maximum sequence. (06 Marks)
c. Write the expression for critical path delay for carry skip and Sklarsky address. (04 Marks)
- 5 a. Explain content addressable memory. (10 Marks)
b. Explain the ideal properties of power distribution network. Also brief on i) 1R drop; ii) L di/dt noise. (10 Marks)
- 6 a. How global clock is generated? Explain it with respect to PLL. (10 Marks)
b. What are the ideal properties of good input/output subsystem? (06 Marks)
c. Write a explanatory note on schedule of IC. (04 Marks)
- 7 a. Explain in detail built-in soft-test technique of testing logic blocks. (10 Marks)
b. Explain the state diagram of test access port (TAP) controller. (10 Marks)
- 8 Write a note on following:
a. Manufacturing test principles.
b. Scannable flip-flops.
c. Gate array and sea of gates design.
d. Faster decoders. (20 Marks)
